

SSCL70N100GS6A

N-Channel Enhancement Mode MOSFET

Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	l _D
100V ±20V	70mΩ@10V	3.2 A	
	100 V	±20V	85mΩ@4V5

Description

The SSCL70N100GS6A is N-Channel enhancement mode MOSFET. Uses SGT Technology and design to provide excellent RDSON with low gate charge. This device is suitable for use in DC - DC conversion, power switch and charging circuit.

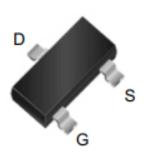
Applications

- Inverter
- DC-DC Converter
- Half and Full Bridge Topology
- Motor Drive Control

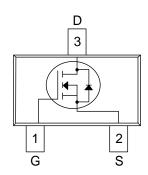
Ordering Information

Device	Package	Shipping
SSCL70N100GS6A	SOT-23-3L	3000/Reel

Pin configuration



SOT-23-3L



Pin Configuration (Top View)



Marking



SSCL70N100GS6A

➤ Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain-to-Source Voltage	100	V
V _{GSS}	Gate-to-Source Voltage	±20	V
l _D	Continuous Drain Current ^a	3.2	А
I _{DM}	Pulsed Drain Current b	12.8	А
P _D	Power Dissipation ^c	1.4	W
TJ	Operation junction temperature	-55~150	$^{\circ}$
T _{STG}	Storage temperature range	-55~150	$^{\circ}$

➤ Thermal Resistance Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance a	80	°C/W

Note:

- a. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with T_A=25 °C. The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}$ =150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

SSC-V1.0 www.sscsemi.com Analog Future



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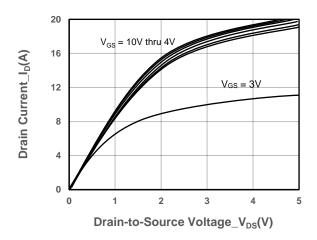
\succ Electrical Characteristics (T_A=25°C unless otherwise noted)

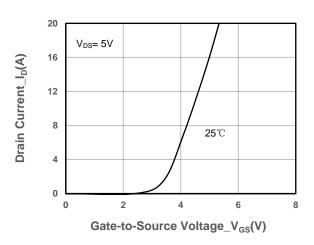
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250uA$	1.0	1.8	2.5	V
Drain-Source On-Resistance	D	V _{GS} = 10V, I _D = 3A		70	95	mΩ
Diain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V$, $I_D = 2A$		85	110	11122
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	lgss	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA
Forward Voltage	V _{SD}	V _G S = 0V, I _S = 3A		0.7	1.3	V
Gate Resistance	R _G	V _{GS} = 0V, f = 1MHz		9.0		Ω
Input Capacitance	C _{ISS}	VDC 50V VCC 0V		171		
Output Capacitance	Coss	VDS = 50V, VGS = 0V, f = 1MHz		58		pF
Reverse Transfer Capacitance	Crss			2.0		
Turn-on Delay Time	T _{D(ON)}			7.0		
Rise Time	Tr	$V_{GS} = 10V, I_D = 3A$		15		
Turn-off Delay Time	T _{D(OFF)}	$V_{DS} = 50V$, $R_G = 3\Omega$		17		ns
Fall Time	T _f			14		
Total Gate Charge	Q _G	V 40V V 50V		3.8		
Gate to Source Charge	Q_GS	$V_{GS} = 10V, V_{DS} = 50V,$		0.9		nC
Gate to Drain Charge	Q _{GD}	I _D = 3A		1.0		
Diode Recovery Time	Trr	I _F =3A, di/dt=100A/us		11		ns
Diode Recovery Charge	Q _{rr}	I _F =3A, di/dt=100A/us		20		nC



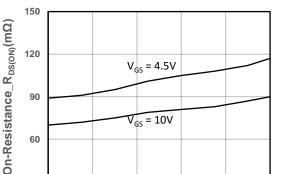


> Typical Performance Characteristics (T_A=25℃ unless otherwise noted)

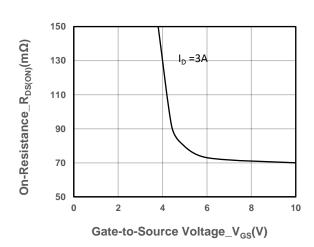




Output Characteristics



Transfer Characteristics



On-Resistance vs. Drain Current and Gate Voltag

Drain Current_I_D(A)

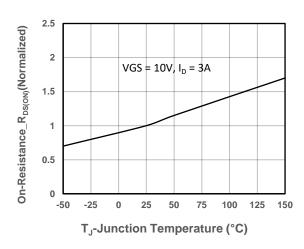
12

16

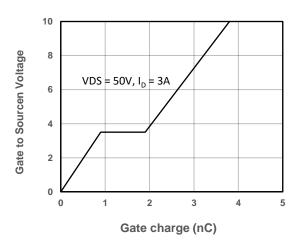
20

30

0



On-Resistance vs. Gate-to-Source Voltage



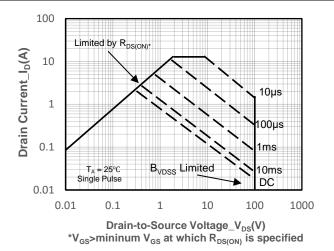
On-Resistance vs. Junction Temperature

Gate-Source Voltage vs. Gate charge

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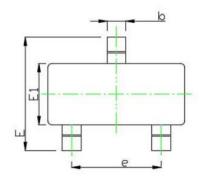


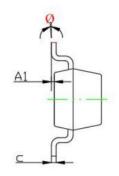


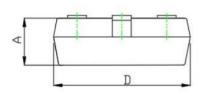
Safe Operating Area vs. Junction-to-Ambient

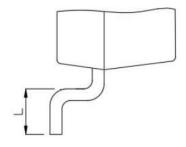


Package Information



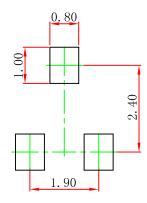






	MILL IMETER			
Symbol	Min.	Nom.	Max.	
Α	0.90	1.00	1.15	
A1	0.01	0.05	0.10	
b	0.35	0.40	0.45	
С	0.08	0.11	0.16	
D	2.80	2.90	3.00	
E	2.25	2.40	2.55	
E1	1.20	1.30	1.40	
е	0.80	1.90	2.00	
L	0.30	0.4	0.5	
θ	0°	/	8°	

> Recommended Pad outline (Unit: mm)







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